```
;PALASM Design Description

;---------------------- Declaration Segment ------------------------------

TITLE     COLOR13 - Pixel Processor
PATTERN   U108 of Control Board
REVISION  1.3
AUTHOR    Joel Tarback, Alen Koebel
COMPANY   ELECTROHOME LTD.
DATE      01/27/93

CHIP  COLOR  PAL22V10 ; --- MUST use Lattice (10 ns) ---

;---------------------- Description ---------------------------------------
;
; This PAL inputs character pixel streams OD (ODDBIT) and EV (EVENBIT)
; from shift registers U88 and U99, as well as XH (XHATCH) from pal
; U117, processes them and outputs digital RGB video. It also inputs
; blanking and clamp signals and outputs several composite blanking
; waveforms.
;
; ODDBIT and EVENBIT are interleaved such that EVENBIT is displayed only
; during the first half of each PIXCLKB cycle and ODDBIT is displayed
; during the second half. Two pixels are therefore output for every clock
; cycle. The pixels are modified by attribute bits which are stored for
; each character. RED-ATT, GREEN-ATT, and BLUE-ATT select the color of "on"
; (binary 1) pixels. These colors are simply the eight possible binary
; combinations of red, green, and blue. The INVERSE and TRANSPARENT bits
; modify the pixels as follows:
;
;          INVERSE  TRANSPARENT  "On" pixels  "Off" pixels
;          -------  -----------  -----------  ------------
;             0          0          black         color
;             0          1        background      color
;             1          0          color         black
;             1          1          color       background
;
; S0 (SELECT0), S1 (SELECT1) and S2 (SELECT2) from register U94 select the
; type of background video to be displayed in the transparent portions
; of the characters. When external video is chosen, the /EXT (INT-EXT)
; output is driven low. This signal controls analog switches on the VIM.
;
; Vertical blanking signal VBL and horizontal blanking signal HBLANK are
; combined with CLAMP (CLAMP-DP) to create BLANK_WFM (BLANK-WFM), which is
; subtracted from the RGB video signals in the output amplifiers (U105,
; U106 and U107). This drives the video to black when a clamping pulse
; occurs and "blacker-than-black" during the rest of the blanking
; intervals. INT-EXT is driven high during the blanking intervals to
; show the internal video and thus blank the display.
;
; CBLANK, created from CLAMP (CLAMP-DP) and VBL, is output to PAL U28.
; If CBLANK is low, U28 will insert wait states into any access made to
; register U94 or RAMs U97, U98 or U102 by the 68000. The read or write
; cycle is thus delayed until CBLANK goes high during a horizontal or
; vertical blanking interval. This prevent "glitching" of the display.
; Design note: CLAMP-DP is used because it occurs inside the true
; horizontal blanking interval. If HBLANK were used, completion of a
; 68000 cycle would glitch the far left side of the display.
;
```